Course Plan

Semester: **4 - Semester**	Year: **2019**
Course Title: **DIGITAL ELECTRONICS**	Course Code: **EC106**
Semester End Examination: **70**	Continuous Internal Evaluation: 30
Lesson Plan Author: Ms. CH SRIDEVI	Last Modified Date: 25-11-2018

Course Outcomes (COs):

At the end of the course the student should be able to:

1. examine the structure of number systems and perform the conversion among different number systems
2. illustrate reduction of logical expressions using boolean algebra, k-map and tabulation method and implement the functions using logic gates
3. realize combinational circuits for given application
4. design and analyses synchronous and asynchronous sequential circuits using flip-flops
5. implement combinational logic circuits using programmable logic devices

Course Articulation Matrix: Mapping of Course Outcomes (COs) with Program Outcomes (POs)

ourse Outcomes (COs) / Program Outcomes (POs)	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**PSO-1**	**PSO-2**
1. examine the structure of number systems and perform the conversion among different number systems	**3**													
2. illustrate reduction of logical expressions using boolean algebra, k-map and tabulation method and implement the functions using logic gates	**3**													
3. realize combinational circuits for given application		**3**		**2**										
4. design and analyses synchronous and asynchronous sequential circuits using flipflops		**3**	**3**											
5. implement combinational logic			**3**											

circuits using programmable logic devices														

Course Content

Content	Hrs
Unit - 1	
Chapter No. 1 - Number Systems and Codes: Review of Binary, Octal and Hexadecimal Number Systems – Conversion methods- complements- signed and unsigned Binary numbers. Binary codes: Weighted and non-Weighted codes – ASCII – Error detecting and Error correcting codes- hamming codes.	8.00 hrs
Unit - 2	
Chapter No. 2 - Boolean Algebra, Switching Functions And Minimization of Switching Functions: Boolean postulates and laws –De-Morgan's Theorem- Boolean function- Minimization of Boolean expressions – Sum of Products (SOP) –Product of Sums (POS)-Canonical forms – Karnaugh map Minimization – Don't care conditions – Quine Mc'Clusky method of minimization, simplification rules. Logic Gates: AND, OR, NOT, NAND, NOR, Exclusive – OR and Exclusive - NOR, Implementations of Logic Functions using basic gates, NAND –NOR implementations.	10.00 hrs
Unit - 3	
Chapter No. 3 - Combinational Logic Design: Definition, Design procedure – Adders-Subtractors - Serial adder / Subtractor - Parallel adder / Subtractor - Carry look ahead adder, BCD adder- Magnitude Comparator- Multiplexer/ Demultiplexer - encoder / decoder parity checker - code converters: Binary to Gray, Gray to Binary, BCD to excess 3 code Implementation of combinational logic using MUX, Decoder.	12.00 hrs
Unit - 4	
Chapter No. 4 - Sequential Circuits: Definition, Flip-Flops- SR Flip flop, JK Flip flop, T Flip flop, D Flip flop and Master slave Flip flops – Characteristic table and equation – Application table– Edge triggering –Level Triggering –Realization of one flip flop using other flip flops – Asynchronous / Ripple counters – Synchronous counters – Modulo – n counter – Classification of sequential circuits –Analysis of clocked sequential circuits: State equation- State table- State diagram –State reduction and State assignment- Register – shift registers- Universal shift register – Shift counters.	12.00 hrs
Unit - 5	
Chapter No. 5 - Programmable Logic Devices: Basic PLD's –ROM, PROM, PLA, PAL. Realization of switching function using	8.00 hrs

PLD's – Introduction to FPGA, CPLD.	

Text Books (List of books as mentioned in the approved syllabus)

1. M. Moris Mano and Michael D. Ciletti, Digital Design, 5th Edition, , Pearson Education, New Delhi, , 2012
2. Zvi. Kohavi, Switching and Finite Automata Theory, Tata McGraw Hill, New Delhi.
3. Gupta BR, Digital Electronics, SK Kataria Publishers, 2009

References

1. John F Wakerly, , Digital Design d Practices, 4th Edition, , Pearson Education., 2008
2. R.P. Jain, Modern Digital Electronics, Prentice Hall of India,New Delhi.

Chapterwise Plan

Course Code and Title: **EC106 / DIGITAL ELECTRONICS**	
Chapter Number and Title: **1 - Number Systems and Codes:**	Planned Hours: **8.00 hrs**

Learning Outcomes:-

At the end of the topic the student should be able to:

	Topic Learning Outcomes	COs	BL
1	compare digital representation of information with the analog representation	CO1	L4
2	understand the fundamentals of converting from one number system to another	CO1	L2
3	Represent numbers and perform arithmetic in bases 2, 8, 10, and 16	CO1	L2
4	Represent signed decimal numbers in 2's complement form, and vice versa	CO1	L2
5	Add and subtract using 2's complement code	CO1	L3
6	Encode symbols and numbers in binary codes.	CO1	L2

Lesson Schedule

Lecture No. - Portion covered per hour	Planned Delivery Date	Actual Delivery Date
1. Introduction to digital systems, Difference between analog and digital systems Applications of digital systems	19-11-2018	

2. Review of number systems Decimal number system,9's and 10's complements, Arithmetic operations using 9's and 10's complements	22-11-2018	
3. Binary, Octal and Hexa Decimal number systems, Conversion methods from one base to another base	23-11-2018	
4. complements- signed and unsigned Binary numbers Weighted and non-Weighted codes – ASCII code	26-11-2018	
5. Binary codes: BCD Code, Gray Code, XS-3 code Applications of BCD, Gray and XS-3 codes	29-11-2018	
6. BCD and XS-3 Addition and subtraction	30-11-2018	
7. Error detecting and Error correcting codes- hamming codes	03-12-2018	
8. Examples on Error Detecting and Correcting codes	06-12-2018	

Review Questions

Sl.No. - Questions	TLOs	BL
1. What is the special relationship between binary, octal, and hexadecimal?	TLO3	L2
2. When hexadecimal number (A4C01)16 is converted to octal and decimal, which representation will require less digits?	TLO2	L2
3. In 2's complement, what do all the positive numbers have in common?	TLO4	L2
4. How is subtraction with 2's complement different from subtraction with 1's complement?	TLO4	L2
5. Gray code representation of (14)10 is	TLO2	L2
6. An 8-bit byte with binary value 10101111 is to be encoded using an even-parity Hamming code. What is the binary value after encoding?	TLO5	L3
7. Test if these code words are correct, assuming they were created using an even parity Hamming Code. If one is incorrect, indicate what the correct code word should have been. Also, indicate what the original data was. 010101100011 111110001100 000010001010	TLO5	L3

Course Code and Title: **EC106 / DIGITAL ELECTRONICS**	
Chapter Number and Title: **2 - Boolean Algebra, Switching Functions And Minimization of Switching Functions:**	Planned Hours: **10.00 hrs**

Learning Outcomes:-

At the end of the topic the student should be able to:

	Topic Learning Outcomes	COs	BL

1	Understand Boolean algebra and basic properties of Boolean algebra	CO2	L2
2	Represent logical functions in Canonical form	CO2	L2
3	apply the laws of Boolean algebra to simplify circuits and Boolean algebra expressions	CO2	L3
4	Apply methods of systematic reduction of Boolean algebra expressions using Karnaugh map and Tabulation methods	CO2	L3
5	Implement functions with NAND-NAND and NOR-NOR logic	CO2	L3

Lesson Schedule

Lecture No. - Portion covered per hour	Planned Delivery Date	Actual Delivery Date
1. Boolean postulates and laws–	07-12-2018	
2. De-Morgan's Theorem- proof	10-12-2018	
3. Logic Gates: AND, OR, NOT, NAND, NOR, Exclusive – OR and Exclusive – NOR.	13-12-2018	
4. Representation of a Boolean function (Truth table, Min term, Maxterm)	14-12-2018	
5. Implementations of Logic Functions using basic gates, NAND –NOR implementations	17-12-2018	
6. Minimization of Boolean expressions – Sum of Products (SOP) –Product of Sums (POS)-	20-12-2018	
7. Canonical forms – Conversion from one canonical form to another	21-12-2018	
8. Karnaugh map Minimization – 2,3&4 variables	24-12-2018	
9. Boolean simplification using Don't care terms	27-12-2018	
10. Quine Mc'Clusky method of minimization	28-12-2018	

Review Questions

Sl.No. - Questions	TLOs	BL
1. State and prove Demorgan theorems	TLO1	L2
2. Simplify the following Boolean expression.	TLO3	L3
3. An automotive engineer wants to design a logic circuit that prohibits the engine in a car from beings started unless the driver is pressing the clutch pedal while turning the ignition switch to the "start" position. The purpose of this feature will be to prevent the car from moving forward while being started if ever the transmission is accidently left in gear. Suppose we designate the status of the ignition switch "start" position with the Boolean	TLO3	L3

variable S (1 =start; 0 = run or off), and the clutch pedal position with the Boolean variable C (1 = clutch pedal depressed;0 = clutch pedal in normal, un pressed position). Write a Boolean expression for the starter solenoid status, given the start switch (S) and clutch (C) statuses. Then, draw a logic gate circuit to implement this Boolean function		
4. Use a Karnaugh map to generate a simple Boolean expression for this truth table, and draw a gate circuit equivalent to that expression: A B C D Output 0 0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0 1 1 0 0 1 0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 0 1 0 0 0 0 1 0 0 1 0 1 0 1 0 1 1 0 1 1 1 1 1 0 0 0 1 1 0 1 0 1 1 1 0 1 1 1 1 1 1	TLO4	L3
5. A car garage has a front door and one window, each of which has a sensor to detect whether it is open. A third sensor detects whether it is dark outside. A security system for the garage follows this rule: the alarm rings if and only if the alarm-switch is turned on and either the front door is not closed, or it is dark, and the side window is not closed Draw the truth table , simplify the expression and construct NAND only circuit which meets the above conditions?	TLO5	L3
6. Obtain minimal expression using the tabular method for the functionF(W,X,Y,Z)= ∑m (0,1,3,4,5,7,10,13,14,15)	TLO4	L3

Course Code and Title: **EC106 / DIGITAL ELECTRONICS**	
Chapter Number and Title: **3 - Combinational Logic Design:**	Planned Hours: **12.00 hrs**

Learning Outcomes:-

At the end of the topic the student should be able to:

	Topic Learning Outcomes	COs	BL
1	design combinational circuits using gates.	CO3	L6
2	Design and implement arthematic circuits.	CO3	L6
3	develop a converter which can convert one binary code to other.	CO3	L4
4	make use of mux, demux in developing the various combinational circuits.	CO3	L3

Lesson Schedule

Lecture No. - Portion covered per hour	Planned Delivery Date	Actual Delivery Date
3. Introduction to combinational logic, Adder-Substractor:Half	31-12-2018	

adder, Full Adder		
8. Half Substractor, Full Substractor	04-01-2019	
1-2. Types of adders: Serial, Parallel,Carry look ahead,BCD Adder	21-01-2019	
4-5. Comparator,Multiplexer,Demultiplexer	24-01-2019	
6-7. Encoder,Decoder	25-01-2019	
9-10. Code Converters:Binary to Grey,Grey to Binary	25-01-2019	
11-12. Design of Code Converters Using MUX and Decoder	03-01-2019	

Review Questions

Sl.No. - Questions	TLOs	BL
1. Design half subtractor using NOR gates only and obtain Boolean expression for difference & borrow.	TLO2	L6
2. Analyse half adder using NAND gates only and obtain Boolean expression for Sum &carry.	TLO2	L6
3. Design the combinational logic circuit using NAND gates only for the following word statement. The insurance policy will be issued to the applicant, if he is: (i) a married female of 22 years or more, or (ii) a female under 22 years, or (iii) a married male under 22 years and who has not been involved in a car accident, or (iv) a married male who has been involved in a car accident, or (v) a married male of 22 years old or above and who has not been involved in a car accident. Design the circuit which can issue the insurance policy to the applicant.	TLO1	L6
4. Develop a code converter that converts a decimal digit from 8, 4, –2, –1 code to BCD.	TLO3	L4
5. Realize the following function of three variables with 8:1 MUX. F (A, B , C) = $\sum$ (7,4,3,1,0)	TLO4	L3
6. Use Multiplexers to implement of Full adder.	TLO4	L3
7. Using 16 X 4 PROM, implement the 4 –bit binary– to– gray conversion.	TLO3	L3

Course Code and Title: **EC106 / DIGITAL ELECTRONICS**	
Chapter Number and Title: **4 - Sequential Circuits:**	Planned Hours: **12.00 hrs**

Learning Outcomes:-

At the end of the topic the student should be able to:

	Topic Learning Outcomes	COs	BL
1	Understand the basic flip-flops	CO4	L2

2	Discriminate Combinational and Sequential Circuits	CO4	L2
3	Interpret Asynchronous and synchronous sequential circuits	CO4	L2
4	Realization of one flip-flop to other flip-flop using excitation table	CO4	L3
5	Analyze the various sequential circuits using different reduction techniques	CO4	L4
6	Design Various counters using flip-flops	CO4	L6
7	Understand various registers and counters	CO4	L2

Lesson Schedule

Lecture No. - Portion covered per hour	Planned Delivery Date	Actual Delivery Date
1. Difference between Combinational and sequential circuits. Latches	28-01-2019	
2. Flip-Flops- SR Flip flop, JK Flip-flop	28-01-2019	
3. T flip-flop, D flip-flop	31-01-2019	
4. Master slave Flip flops – Characteristic table and equation	01-02-2019	
5. Application table– Edge triggering –Level Triggering	04-02-2019	
6. Realization of one flip flop using other flip flops	04-02-2019	
7. Asynchronous / Ripple counters – Synchronous counters	07-02-2019	
8. Modulo – n counter	08-02-2019	
9. Classification of sequential circuits	11-02-2019	
10. Analysis of clocked sequential circuits: State equation- State table	11-02-2019	
11. State diagram –State reduction and State assignment	14-02-2019	
12. Register – shift registers- Universal shift register – Shift counters	15-02-2019	

Review Questions

Sl.No. - Questions	TLOs	BL
1. Explain SR Flip-flop using Truth table	TLO1	L2
2. Design a 3-bit synchronous binary counter using T flip flop.	TLO6	L6
3. Convert JK Flip-Flop into SR Flip-Flop.	TLO4	L3
4. Draw the circuit diagram and explain with wave forms 4-bit Asynchronous binary ripple counter.	TLO3	L2
5. What is a Shift register? Briefly explain about Universal shift register with neat sketch.	TLO7	L2

6. Minimize the table using Partition technique and draw its State diagram. PS NS X=0 X=1 A E,0 D,1 B F,0 D,0 C E,0 B,1 D F,0 B,0 E C,0 F,1 F B0 C,0	TLO5	L4
7. What is meant by Race around condition in JK flip-flop and how to avoid explain with diagram.	TLO1	L2

Course Code and Title: **EC106 / DIGITAL ELECTRONICS**	
Chapter Number and Title: **5 - Programmable Logic Devices:**	Planned Hours: **8.00 hrs**

Learning Outcomes:-

At the end of the topic the student should be able to:

	Topic Learning Outcomes	COs	BL
1	Understand the concepts of programmable logic devices.	CO5	L2
2	clasify between various logic devices such as ROM,PLA,PAL	CO5	L2
3	Design and Implement Combinational circuits using programmable logic devices.	CO5	L6

Lesson Schedule

Lecture No. - Portion covered per hour	Planned Delivery Date	Actual Delivery Date
1-2. Basic PLDs: ROM, PROM, Functions devices Realising using ROM, PLA, PAL	21-02-2019	
3-4. Realisation of Switching Functions using PLA	22-02-2019	
5-6. Realization of Switching Functions using PAL	25-02-2019	
7-8. FPGA, CPLDs	28-02-2019	

Review Questions

Sl.No. - Questions	TLOs	BL
1. What are Programmable array logic (PAL) devices? What is the difference between FPLA and PAL devices?	TLO1	L2
2. Implement a excess – 3 to seven segment decoder using PLA of proper specification.	TLO3	L6
3. Using the PAL implement the following SOP functions of 4 variables. X0 = A·C · D + A· B · D + A· B ·C · D + A·C · D X1 = A· B ·C · D X 2 =	TLO3	L6

A + C · D + A·C X3 = B ·C + A· B + A· D + B · D		